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## AMENDMENT TO THE CLAIMS

1. (Currently amended) An integrated circuit comprising:

at least two logic circuits including a first logic circuit and a second logic circuit having the same function as said first logic circuit; [[and]]

a direction circuit for directing operation or halt of said first and second logic circuits; [[,]]

a first output circuit for receiving an output of said first logic circuit;

a second output circuit for receiving an output of said second logic circuit; and

one signal line for simultaneously receiving both the outputs of said first and second output circuits,

wherein said direction circuit directs, in normal mode, the operation of one of said first and second logic circuits based on an externally supplied select signal, and directs, in testing mode, simultaneous operation of said first and second logic circuits when said select signal is a signal for selecting said first or second logic circuit, and

wherein said first and second output circuits enter an enable state in response to an externally supplied testing mode signal.

2. (Canceled)

3. (Original) The integrated circuit of claim 1, wherein each of said first and second logic circuits performs a logic operation corresponding to a function according to an externally supplied function signal when the operation thereof is directed by said direction circuit.

4. (Currently amended) A testing method for an integrated circuit composed of: at least two logic circuits including a first logic circuit and a second logic circuit having the same function as said first logic circuit;

a first output circuit for receiving an output of said first logic circuit;

a second output circuit for receiving an output of said second logic circuit; and

one signal line for simultaneously receiving both the outputs of said first and second output circuits,

said method comprising the steps of:

simultaneously operating said first and second logic circuits;

transferring outputs of said first and second logic circuits to said one signal line;

measuring a supply current flowing through said one signal line; and

determining whether said first and second logic circuits are defective or nondefective based on said measured supply current.

5. (Previously presented) The integrated circuit of claim 1, wherein the direction circuit is connected to said at least two logic circuits.

6. (Previously presented) The integrated circuit of claim 1, further comprising a current measuring unit, wherein the outputs of the first and second logic circuits are transferred to one signal line, and wherein said current measuring unit measures a supply current flowing through the signal line to determine whether the first and second logic circuits are defective or nondefective.